Does Ultrasonic Cleaning of PCBs Cause Component Problems: An Appraisal

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Abstract

An investigation of the use of ultrasonic agitation for cleaning printed circuit boards using CFC-based solvents has shown that under the standard conditions required to produce clean assemblies, no damage will occur to the components studied. Damage can only be induced by use of anomalously longer times or higher power densities. In all cases in which damage has been induced, it is of a purely mechanical nature due to fatigue, and is located on the device bond-wires and/or the package legs. Cleaning using CFC-based solvents under standard ultrasonic conditions of power density and time etc., is readily achieved within 2 minutes, even with a minimum standoff heights. The preliminary results obtained using aqueous and semi-aqueous solvents support the apparently benign nature of the ultrasonic agitation in causing component damage.

1.0 Introduction

It has long been recognized that effective cleaning of printed circuit boards (PCBs) presents a major problem, especially with the advent of surface mount technology (SMT) and more complex package types. One of the most effective means of cleaning PCBs, especially under components where excess flux and flux residues are held by capillary action, is to subject them to ultrasonic agitation, and its use has been supported [1,2] for many years. Indeed, the technique is used routinely in many market sectors. However, in the past, it has been suggested that the ultrasonic process might give rise to irreversible damage in the devices and soldered joints, and/or to long term reliability problems. The two major effects to the components themselves were expected to be breaking of internal bond wires as a result of forced vibration (possibly exacerbated by resonance effects determined by lead length and ultrasonic frequency), and fatigue fractures of the legs or soldered joints.

On these grounds the use of this technique in the military context has been effectively prohibited [3,4]. These worries appear to have been based on early work [5,8] in which the data were obtained using now obsolete ultrasonic equipment operation at 25 kHz, and on devices and boards of old technologies (including germanium transistors). Since those early papers, there has been a dramatic improvement in the situation, with the introduction of improved bonding technologies, a general change to aluminum bond wires, a much tighter distribution of both bond strengths and quality of joints, and replacement of ultrasonic cleaners with new equipment operating at about 40 kHz. However, apparently adverse reports have appeared [9,10] relatively recently.

On the other hand, extensive evaluations of failed components at the Hirst Research Centre have not provided any unambiguous data supporting the notion that sensibly used ultrasonic agitation causes component problems. However, they have shown that it would highlight component quality problems (e.g. by enlarging pre-existing micro-cracks in passive components, detaching unsatisfactory bonds). The evidence in the literature is both scant and ambiguous. So the question to be addressed was clearly, "Does ultrasonic agitation damage components?"

In an attempt to assess the current situation, therefore, a program has been carried out to obtain data relating to potential degradation of the device and/or the soldered joint. The program concentrated in two complimentary topics: the identification of any physical damage leading to device malfunction resulting from exposure to ultrasonics (the major topic), and the efficiency of cleaning using ultrasonic techniques (the secondary objective). The purpose of this paper is to report briefly the results of the investigation.

2.0 Objectives

The program has comprised two tasks. The first, which has now been essentially completed, was to explore the effect of ultrasonic agitation using CFC solvents, since these are extensively used in the industry at the present time. The second task comprised a study of the use of aqueous and semi-aqueous solvents (likely CFC replacements for some applications). In both tasks the main aims were as follows:

(a) to identify the type of nature of any damage induced in a chosen range of components by ultrasonic agitation using CFC-based solvents.

(b) to assess the damage in those components and determine the effects of exposure time and power density on the accumulation of damage.

(c) to assess the regimes of safe ultrasonic operation consistent with adequate cleaning.

3.0 Task Investigation

3.1 Equipment and Components Used

The full program schedule has been described elsewhere [10,11]. However, in order to reduce sensibly the "cleaning matrix" and to provide useful data in an acceptable timescale, a number of decisions were made at the outset:

(i) to concentrate on obtaining data relating to any component damage, and not on aspects of cleaning;

(ii) to use state-of-the-art equipment which is currently used in the industry;

(iii) to use only one frequency i.e. 38 kHz which is industry standard and extensively used; lower frequencies are known to cause cavitation damage more readily, and hence are rarely used, and higher frequencies (e.g. 100 kHz) are seldom used for cleaning operations;

(iv) to use a range of components typical of that used in the industry i.e. not to attempt to identify those that might be most prone to damage on the basis of unproven hypotheses;

(v) to use only one representative CFC solvent (i.e. Arklone AM), since the primary topic was the study of damage accumulation and not aspects of cleaning. It was expected that the acoustic properties of CFC solvents would show little variation form each other.

With the full cooperation of the suppliers, two different ultrasonic cleaning units have been used, both operating at 38 kHz: an ICI Cleanline 2 type R2818UV28, and a Kerry KS 451 tank with a class D driver unit with variable power output. Both are state-of-the-art machines typical of those used in the microelectronics industry. The ICI machine operated at a mean output electrical power density of about 11 watts/litre, while the Kerry machine was capable of operation over a range of power densities with a maximum of 32 watts/litre. Package component types used in this investigation were: ICs in DIL packages, both plastic and ceramic in large and small sizes; SOICs; PLCCs; pin grid arrays; SOT-23 diodes; SM LEDs; chip resistors and capacitors; and TO-18 packaged transistors. All the components used were from batches qualified to either MIL or commercial standards. Examinations were carried out on examples of the as-received components to ensure that the quality of the components was consistent with their purchase specifications, and that any failures would not be due to questionable quality. The components were stressed in three ways, as appropriate:

(i) mounted on test boards designed and fabricated to accommodate a range of representative leaded and SM components (active and passive). The architecture of this board was designed to allow self-diagnosis.

(ii) mounted on boards to give large numbers of the same device type on a particular board.

(iii) loose in a basket in the ultrasonic tank, in order to increase markedly the stress and, therefore, damage for a given exposure, and hence gather more information about the type of damage and its statistical distribution.

3.2 Assessment Techniques Employed

Assessment of the damage accumulation was made using essentially electrical techniques and the self-diagnosing test board [11,12]. The nature and type of the damage and its generation were established using a range of analytical and microscopical techniques as appropriate. In order to assess the effect of ultrasonic agitation on weakening bond strengths, and hence on the possibility of compromising future field life, the strengths of many (>5000) bonds have been measured. The individual wire-bond strengths were measured using a specially designed and built bond-wire puller (a modification of a GEC Meniscrograph wetting balance solderability tester), which provided not only the ultimate failure strength, but also a complete stress-strain curve for every bond studied. In addition, in order to explore the possibility that the ultrasonic agitation may have been inducing incipient damage that would have manifested itself in later life leading to poor field performance, accelerated testing was undertaken. Many devices were baked at 150°C for 124 hours, following 10 hours exposure at high power densities.

For cleaning studies, glass slides mounted onto a special flux test board with interdigitated patterns were used allowing both surface conductivity and visual inspection to determine the degree of cleanliness. Moreover, following removal of the slides, analytical measurements of the cleanliness of both the slides and the corresponding areas on the board were undertaken using Fourier transform infrared (FTIR) and X-ray photoelectron spectroscopic (XPS) techniques.

4.0 Task 1 Results and Discussion

It became clear at an early stage of the investigation that present day components are robust and difficult to damage using ultrasonic cleaning techniques under normally acceptable exposure times and power densities (a few minutes at 10-11 watts/litre). In order to significantly stress the components, much of the work has been undertaken using power densities (up to 32 watts/litre) and times (greater than 100 hours) considerably in excess of those normally used for effective cleaning of PCBs. The relationship between power density and damage rate has also been investigated.

4.1 Individual Component Types

4.1.1 TO-18 Transistors

These devices were stressed both soldered to circuit boards and lying loose in a wire cage, for periods up to 100 hours and power densities up to 32 watts/litre. The results clearly demonstrated that even with high power density long term exposure was required to damage these components.

For example, at normal power density exposure (11 watts/litre) it has not proved possible to cause damage in TO-18 transistors after continuous exposure for 27 hours. However, damage could be induced in shorter periods at high power densities, and Figure 1 shows the cumulative failure percentage for both mounted and loose TO-18 transistors plotted against exposure time. The curve for the loose devices consists of three separate portions, a central linear region bounded by two curved regions. It was suspected that these regions comprised separate populations of failures and an attempt was made to separate them. In Figure 2, group A consists of the first three points (for loose components) from Figure 1 plotted on the assumption that they represent a population containing 8 out of the 100 transistors. Group B likewise consists of the next 15 failures and represents the central portion of Figure 1. The other 77 devices, group C, comprise a third distribution in which 2 failures had occurred after 70 hours, and no further failures up to 100 hours (i.e. the time to 3 failures was greater than 100 hours). The distributions A and B lie on reasonably straight lines, the A population consisting of transistor bonds which are the easiest to break with a mean life of about 1.5 hours, and the B distribution being more robust with a mean life of about 25 hours. However, the majority of the devices (77%) have a very long life (only 2 having failed at 70 hours, and no more at 100 hours), implying a mean life for this distribution of greater than 1000 hours.

In all cases, examination of the failed bond wires confirmed that failure had occurred, as expected, at the heel of the bond due to mechanical fatigue. The sites of the failure were at either the wire-bond to pad joint (see Figure 3), or at the wire-terminal post joint.

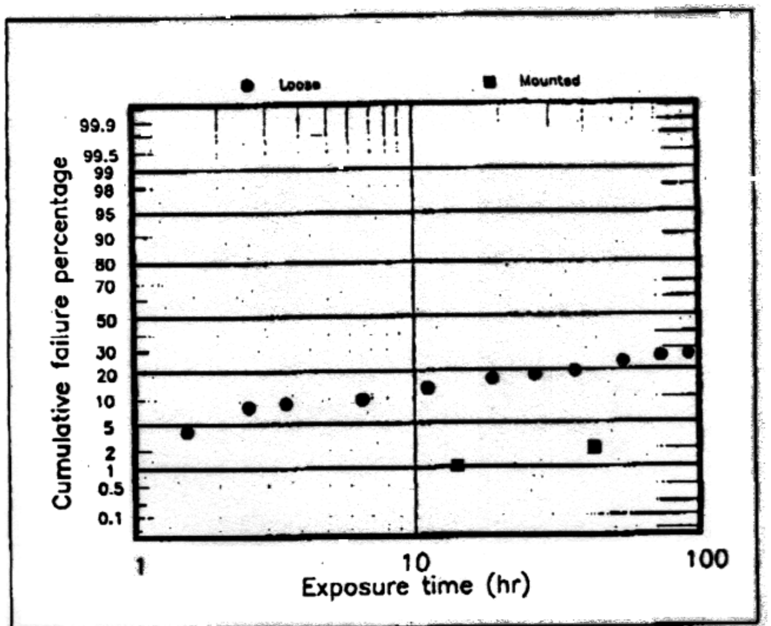


Figure 1 Failure of TO-can transistors at high power density

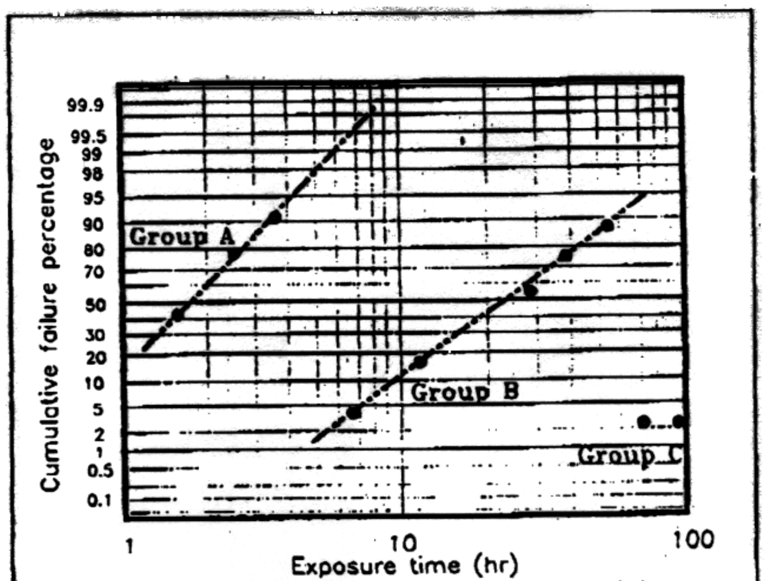


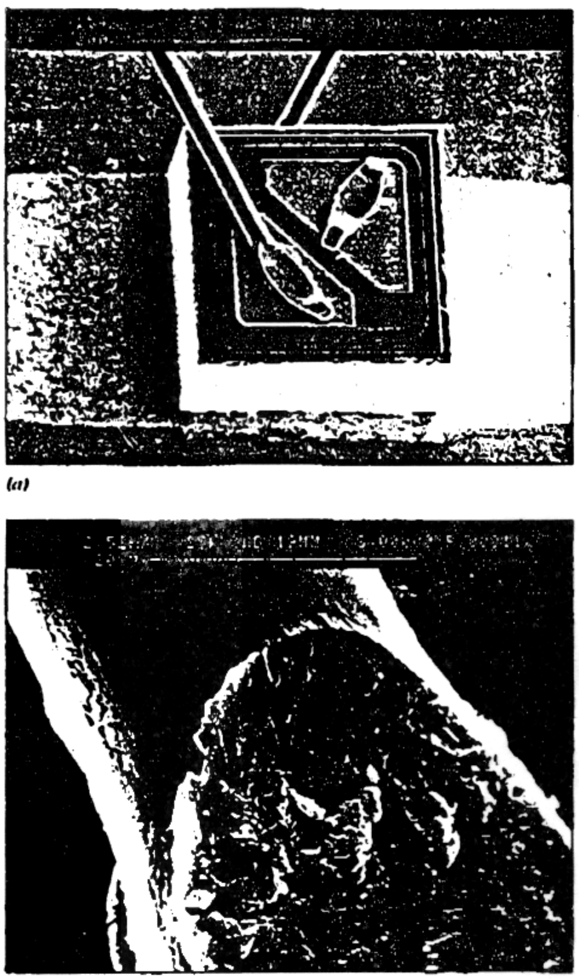
Figure 2 Failure of TO-can transistors at high power density

4.1.2 Plastic DIL Devices

DIL packaged devices were stressed in a similar manner to the TO-18 transistors. Not unexpectedly the devices proved even more robust, since the bond leads are held captive by the plastic molding. No failures of bond leads were encountered at normal power densities for exposure times up to 100 hours, or at high power densities for test periods of up to 25 hours. It was noted, however, that many legs on board-mounted ICs subjected to the higher power densities had been damaged to varying degrees including in some cases complete breaks. Further work was, therefore, initiated to examine the damage to the legs and its genesis. Twenty 74LS47 ICs were mounted onto each of 2 boards and exposed for up to 4 hours, one at normal and one at high power densities. After 0.5, 1, 2, and 4 hours, five ICs were unsoldered and carefully examined using an SEM. Damage of the legs was evident, and could be conveniently, though not rigorously, classified into four levels.

broken—a complete break
major cracks—a significant crack
minor cracks—just visible
no cracks—no visible damage

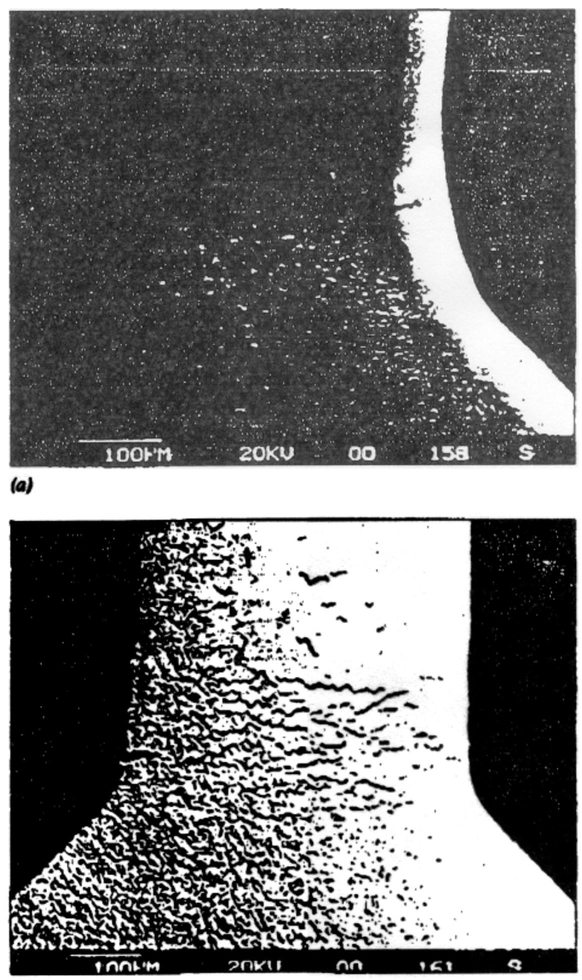
Typical micrographs are shown in Figure 4, and it is evident that erosion of the leg material had taken place typical of that expected from cavitation damage. The results demonstrated that although little significant damage to the IC legs will occur for times up to 4 hours at normal power density, some damage is induced after half an hour at high power density (see Figure 5).



(a)

(b)

Figure 3 (a) and (b) SEM micrographs showing typical fracture of wire bond



(a)

(b)

Figure 4 (a) and (b) SEM micrographs illustrating progressive fatigue damage on legs of DIP devices

4.1.3 Ceramic DIL Devices

In ceramic packaged devices, the internal bond wires between the package legs and the silicon chip surface are free to vibrate: hence it is possible that damage could occur. Consequently, both small (4116-type 18 pin RAM and 4001-type 14 pin CMOS) and large (27C256 28 pin EPROM) packaged CMOS devices were subjected to ultrasonic agitation, and two essentially different measurement schemes were used to assess the damage.

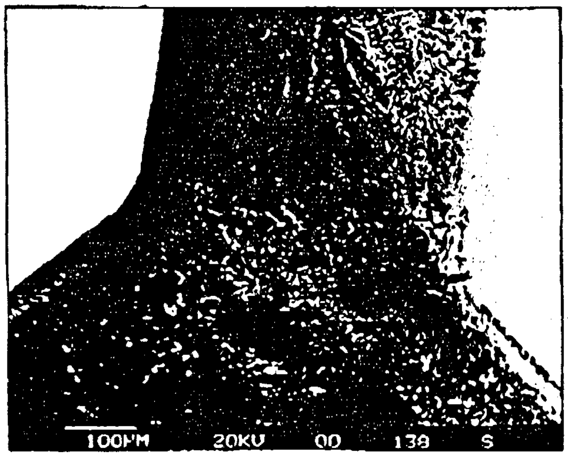
For 4001 CMOS and 4116 RAM devices, ten at a time were mounted onto boards which were then ultrasonically stressed for various periods of time. Electrical testing showed that while the 4001 parts did not exhibit any damage after 100 hours exposure (i.e. no bond wire had been broken), some failures were encountered with the 4116 parts. Subsequently, the devices were delidded and the strengths of a large number of bonds measured. The resulting bond strength distributions were then compared with similar distributions for virgin devices. Figures 6 and 7 present the distributions for the virgin 4001 and 4116 parts respectively. All the bonds are above the specification value [13] of 1.8 gm for the 30 μm diameter aluminum wires of these devices.

The bond strength results for the stressed 4001 devices reflected the electrical measurements (i.e. no zero gram failures, and no statistical change from the virgin bond strength distribution), although a single bond (0.7%) failed at 1.8 gm after 100 hours. The 4116-type memory devices, however, did incur failures of the bond wires at times greater than one hour (at high power densities) rising to about 10% at 100 hours. Figure 8 shows the distribution for these devices after 100 hours stress. It may be conjectured that there is a subpopulation of intrinsically weak bonds within the population of virgin devices, and that these fail during the ultrasonic agitation. The fact that the distribution of non-failed bonds after stressing was identical to the initial distribution indicates that the bond failures occur randomly in the initial distribution; it is not a subset of weaker bonds that is failing. The implication of these results is that the factor affecting susceptibility to failure is not apparent in the initial bond strength distribution; it may be related to the surface condition of the wire (nicks, etc.), or it may be related to bond position within the package, the corner bonds being more prone to failure. However, these 4116-type devices were about 10 years old, and although many similar devices are still in use, they are not representative of present-day quality. But the lead lengths and diameters are similar to those of the 4001 series devices, so there should be no difference in geometrical terms.

The cumulative failure percentage for mounted 4116-type devices for strengths <1.8 gm is shown in Figure 9 as a function of exposure time at high power density. It is evident that there are two (essentially straight line) sections—the failure rate increases from zero at 6 minutes to about 10% after one hour, and thereafter (at least to 100 hours) remains approximately constant. Using the scaling factor of 1000 (see Section 4.2 below) implies that no failures would be incurred after 100 hours exposure at standard power densities.

An additional set of data was gathered for unmounted 4116-type devices i.e. loose in a basket in the ultrasonic cleaning equipment. In this case the "constant" percentage failure regime (i.e. 10%) had already been reached by six minutes, and still continued to 100 hours (see Figure 9). The fact that the "constant" level was the same for both captive and loose devices implies that the failure mechanism was the same in both cases. The difference between the loose and captive devices was that in the former case the susceptible bonds were eliminated faster. However, whether in loose or captive devices the other bonds remained unaffected.

There was clearly a difference between the 4116- and 4001-type devices in terms of the damage accumulation, although



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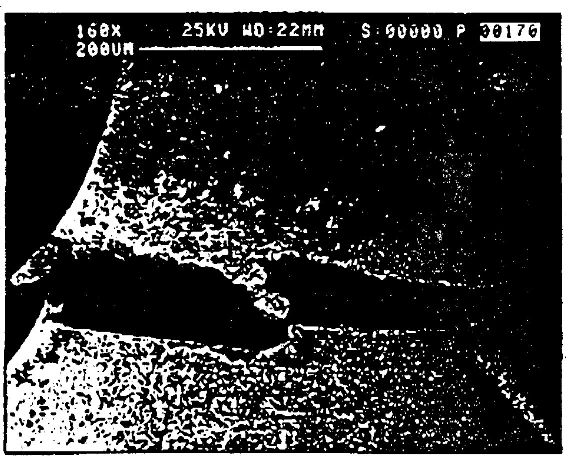

(d)

Figure 4 (c) and (d) SEM micrographs illustrating progressive fatigue damage on legs of DIP devices

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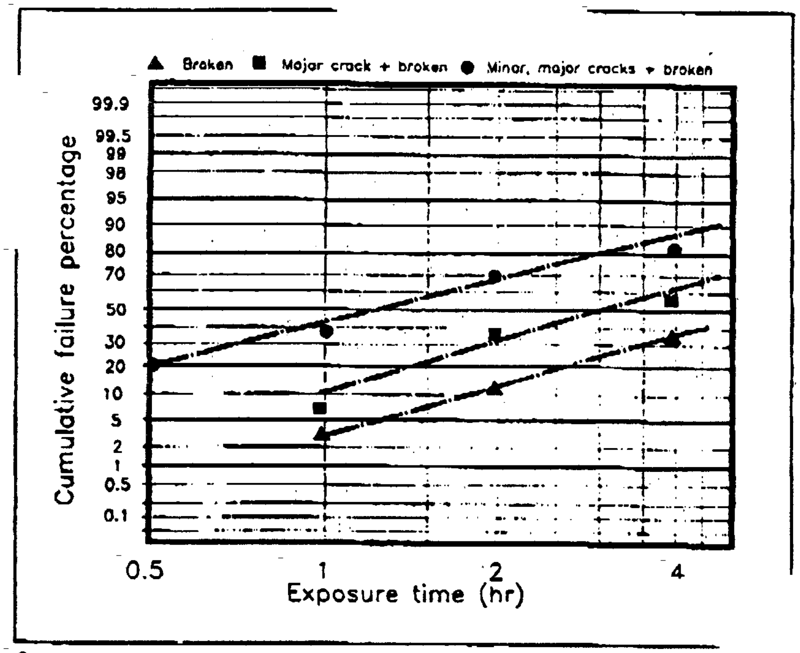

Figure 5 Damage to DIL legs at high power density

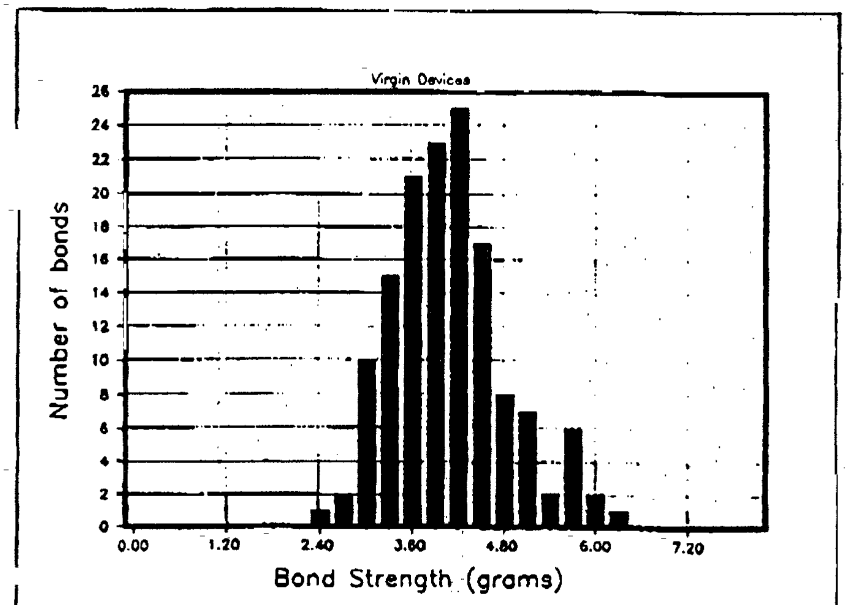

Figure 6 4001 bond strength distribution

they had similar virgin bond strength distributions; hence, the difference is thought to be unrelated to the bond strength per se, but is a function of another characteristic of the bond wire which makes the older devices more susceptible. It is clear from the morphology of the damage that the failure was due to fatigue which had been initiated at surface defects at high stress regions; these would not affect the pull strength of good devices, but could make bonds susceptible to ultrasonic damage.

4.1.4 EPROM Devices

The EPROMs were preloaded with code such that the integrity of each pin could easily be measured by reading out the contents of the devices. Although boards containing ten EPROMs were stressed at both normal and high power densities for periods up to 100 hours, no damage was evident and all the devices continued to work satisfactorily.

4.1.5 Plastic SOIC Devices

Plastic encapsulated SOIC devices (in 16-pin narrow body packages with gull-wing leads) stressed for up to 8 hours at high power densities on a PCB, displayed the same behavior as plastic DIL packages i.e. some cracking of the legs but no internal damage. Again four levels were used to assess this cracking ranging from no visible damage to a complete break (see Figure 10), but the level of damage for a given exposure was much less than that experienced by the larger DIL packages, and for short times no significant amount of damage had been incurred.

4.2 Effect of Ultrasonic Power Density

To gain a fuller understanding of the damage induced at high power densities, the variation of damage with power density was studied using loose transistors since these had proved to be the devices most sensitive to damage. Power densities of 32 watts/litre, 26 watts/litre and 16 watts/litre were used, and the time required to produce a given failure rate measured.

From the previous data a 7% failure rate was chosen as representing the linear failure rate region. A log-log plot of time to failure against power gave a straight line (see Figure 11), and extrapolating this to 11 watts/litre (the power density normally used in cleaning PCBs) gave a time of 2000 hours for 7% damage compared to 2 hours at the high power density used in this study. Hence the power density/time relationship is such that for a factor of 3 increase in power density, the time required to accumulate the some level of damage is reduced by a factor of 1000. The only other components for which failures were obtained at both normal and high power density were the SM LEDs. The relevant data are included in Figure 11 and indicate that the acceleration factor of 1000 is again appropriate, although the two types of devices were radically different, as were the modes of failure rate.

4.3 Test Boards

These boards, which contained a mix of surface mount and through-hole components, were designed to be essentially self-diagnosing [11,12]. By exercising the microprocessor devices (in three different packages—DIL ceramic, J-leg plastic, and PGA ceramic) via an off-board EPROM, it was possible to determine whether any of the bond wires were broken: each lead was monitored by a pair of LEDs and their status during the electrical testing of the board contained the information required.

4.3.1 LEDs and SOT-23 Devices

A selection of boards was exposed at both normal and high power densities for times up to 124 hours: boards stressed for times less than 15 hours were exposed singly, while the other boards were stressed three at a time. The apparently benign effect of normal power density operation was again confirmed, the only adverse effects being that an average of 0.5% SM LEDs were detached (at the solder joints) from the boards exposed for 124 hours. However, more serious damage could be induced by increasing the power density to 32 watts/litre, after which many LEDs and SOT-23 diodes sheared off at their legs. As an example, a plot of the cumulative damage for the LEDs is shown in Figure 12 as a percentage of the total number of mounted LEDs. The fact that these devices proved to be the most fragile parts of the boards essentially precluded the use of on-board electrical assessment to determine failure.

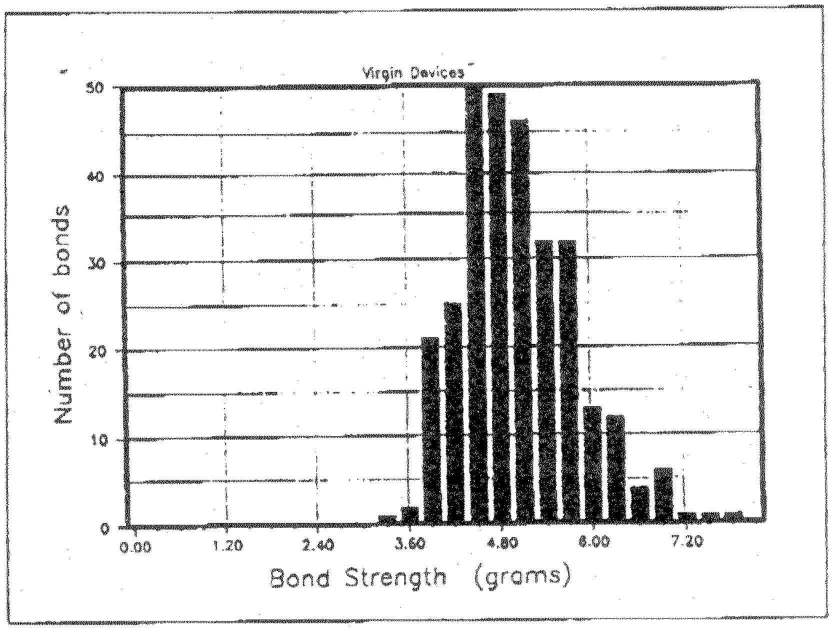

Figure 7 4116 bond strength distribution

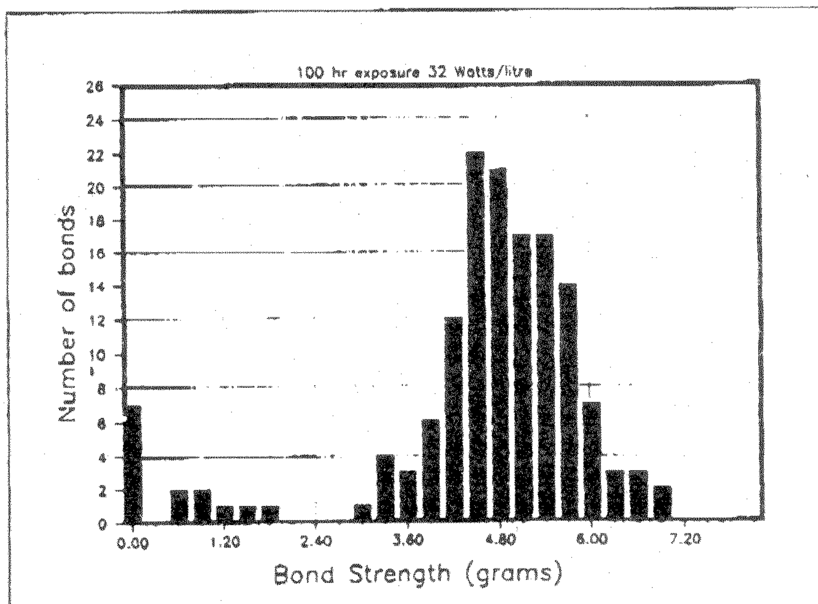

Figure 8 4116 bond strength distribution

4.3.2 Passive Devices

Even at the high power density many components remained unaffected. For example, there were never any failures of the chip capacitors or chip resistors: the failures were confined essentially to the LEDs and SOT-23 packages or to metal lidded devices which exhibited occasional loss of hermeticity.

4.3.3 68000-type Microprocessors

On each board the two ceramic packaged 68000-type devices were opened and bond pull strengths measured for all bonds. Under normal power density conditions there were no broken bonds and the bond strength distributions remained unaltered. Under high power density conditions a small number of bonds had failed after 124 hours, and the results were similar to those for the 4116-type devices. In terms of damage accumulation, as with the 4116 data, there were two sections to the curve (see Figure 13); an initial portion in which the failures rise from 0.7% after 10 minutes to about 5% after 30 minutes, and a second portion remaining essentially unchanged up to 100 hours. From this data and the power scaling factor of 1000:1, it is predicted that at normal power densities 0.7% failures would occur at about 170 hours.

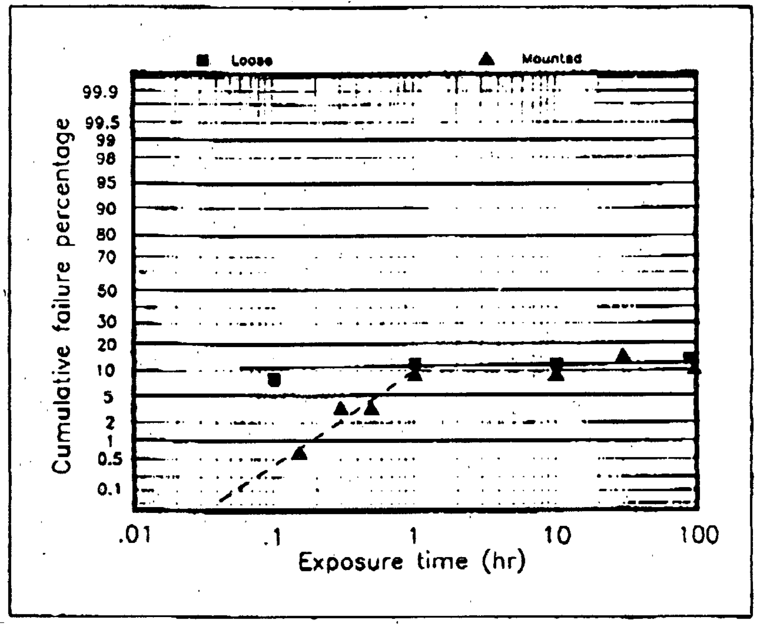

Figure 9 Failure of 4116 devices at high power density

4.4 Accelerated Testing

In order to explore the possibility that the ultrasonic agitation could give rise to incipient damage with consequential degradation of field performance, accelerated tests have been carried out. There are two broad categories of accelerated tests: those based on a thermal stress and those which give rise to a mechanical stress. Since the exposure to ultrasonic agitation gives rise to mechanical effects, further mechanical stress would only continue the same process, and generate no new information. Hence, although it was considered unlikely that any thermally activated failure processes were involved, for completeness a thermal exposure stress exercise was undertaken. A group of the 4116-type RAM devices were baked at 150°C for 124 hours following 10 hours exposure at high power densities, but no change in the bond wire strength distribution was observed at any stage (virgin; after ultrasonic exposure; after accelerated testing).

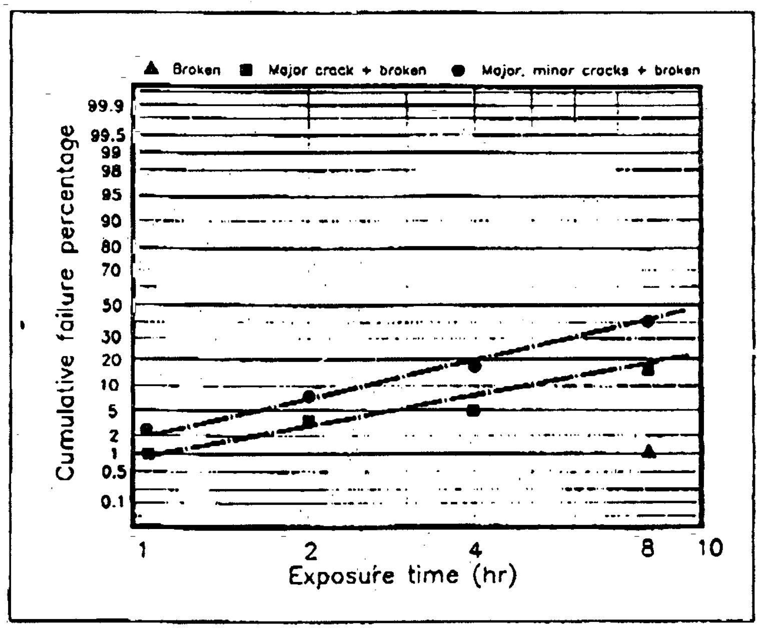

Figure 10 Damage to SOIC legs at high power density

4.5 Efficiency of Cleaning

To assess the efficiency of ultrasonic agitation for cleaning fluxes from PCBs a simple test board with interdigitated combs to facilitate measurement of surface insulation resistance (SIR) was used. Structures for cleaning trials were made by coating the boards with a flux, covering the flux with a square glass slide spaced from the board with C-shaped shims, and passing the assembly through an IR reflow machine with known temperature profile. The boards were cleaned under standard power density exposure for various times, the cleanliness being assessed in-situ both visually and using SIR measurements, and after removal of the glass slide using several analytical techniques.

A series of fluxes (RMA 6381/35, SA701 and RA PC29/17) was used and in all cases cleaning was effected in less than two minutes. Trials to ascertain cleaning time as a function of standoff height (from touching to 0.005") for the hardest of the fluxes to remove (RMA 6381/35) were conducted after passing each board twice through IR reflow to ensure a worst-case condition. Again cleaning under standard power density conditions was complete within two minutes even for the minimum standoff height used. The results, which are presented graphically in Figure 14 with corresponding results generated [14] with and without ultrasonic agitation, are in broad agreement with those of other work.

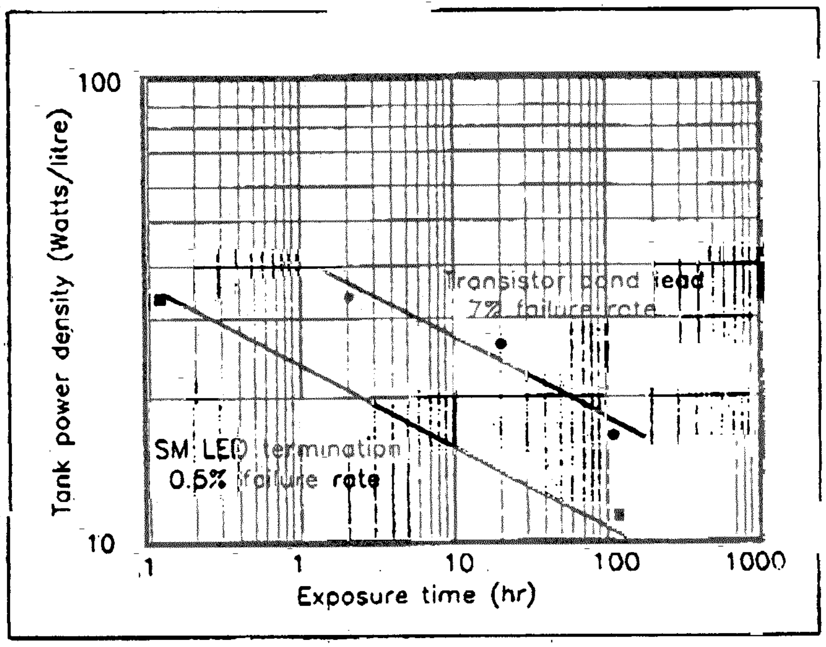

Figure 11 Time to failure vs. tank power density

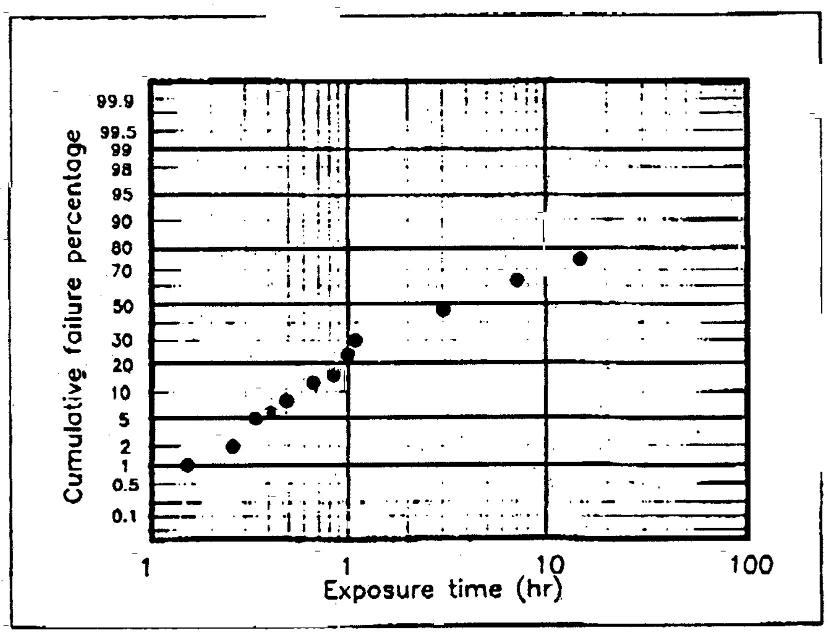

Figure 12 Failure of SM LEDs at high power density

4.6 Resonance

It is often assumed that the leads within integrated circuits exhibit a significant resonance at an appropriate frequency, which depends on lead length and material. Hence, it has been suggested that at a given frequency this resonance may give rise to early bond wire breakages. Calculation of the resonant frequencies to be expected in the absence of any damping have been carried out [15,16] by a number of workers (including the authors) based on vibrating beam theory. These calculations indicate that for both Al and Au wires (diameter 30 μm) the resonant frequency is <10 KHz for lead lengths of approximately 3 mm, the latter being the maximum length encountered in the packages used in this study.

Attempts were made to observe resonance occurring in bond wires of this length using a vibration table driven at variable frequency (up to 10 kHz) and constant amplitude. The device leads were viewed in a microscope using stroboscopic illumination whose frequency was set slightly different from that of the table such that the vibrational amplitude could be observed. No resonance was detected in this experiment, the amplitude of vibration being essentially constant over the sweep frequency range. An alternative method of observing resonance using a mechanical impulse technique was also employed, in which an r.f. signal was applied to the bond wire and the capacitatively coupled signal from the metal package lid was monitored for amplitude modulation during (and following) each mechanical impulse. The resultant signal was of short duration and showed no sign of resonance (i.e. the logarithmic decrement was significantly shorter than the period of vibration of the wire).

That no resonance occurred is not surprising in view of the fact that for both Al and Au the internal energy losses are high and hence their mechanical Q-factor is low. This is particularly true for bond wires since they will have been fully annealed by the package sealing heat-treatment (>400°C for CERDIP packages). On the other hand, long wires, because of the higher ratio of inertia to stiffness, are capable of larger amplitude of vibration for a given energy input. This larger amplitude can give rise to large strains at the point of bond attachment. Large strains associated with long wires (compared to short wires) may result in the elastic limit of the wire being exceeded, leading to fatigue failures. This is the situation thought to occur in hybrid packages, and may explain the sometimes reported extreme sensitivity of hybrids to the ultrasonic vibration (not examined in this work).

Whether or not resonance (or high amplitude vibration) occurs, the failure mode will be the same: fatigue at the high strain site on the bond attachments, as displayed in Figure 3.

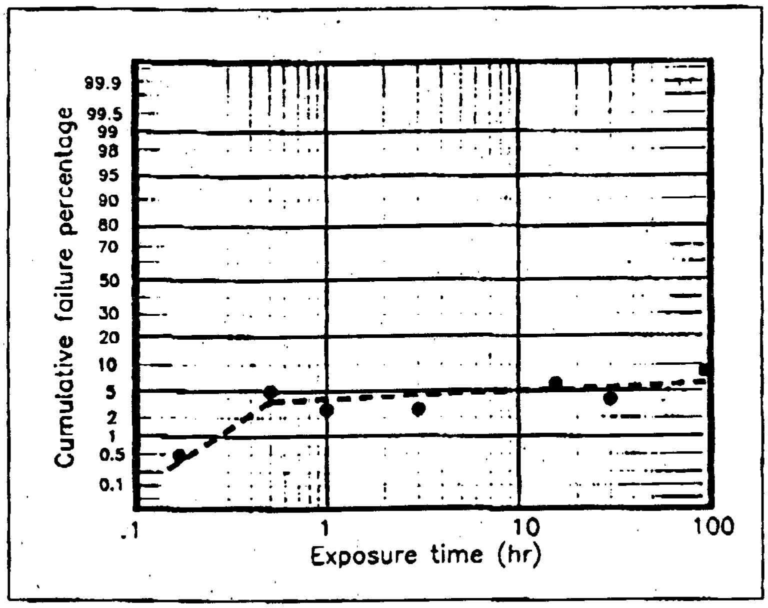

Figure 13 Failure of 68000 DIL devices at high power density

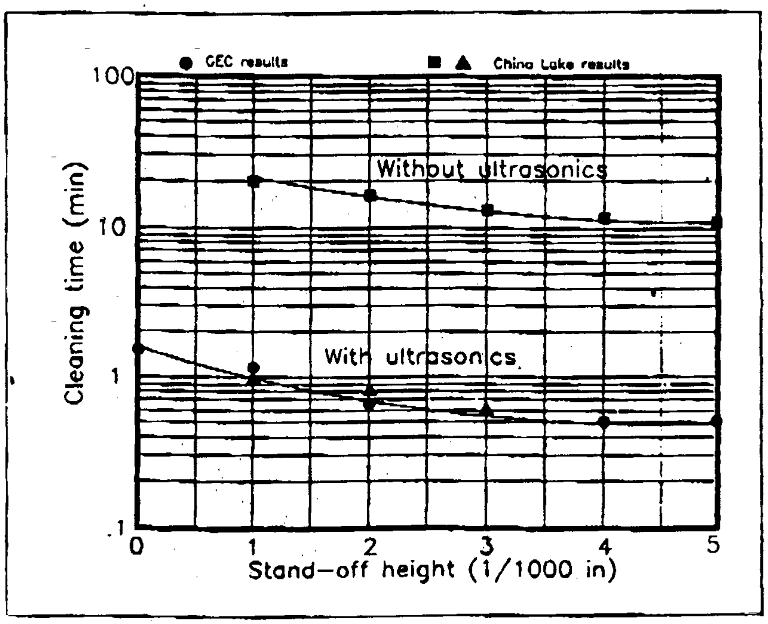

Figure 14 Cleaning time as a function of standoff height

5.0 Task 1 Conclusions

For potential users of ultrasonic cleaning of PCBs, the findings of this work are encouraging, and suggest that there is a large margin of safety when employing currently accepted regimes of operation. This safety margin is shown schematically in Figure 15. The results relate only to the range of components studied, and a summary of the damage observed on these components is given in Table 1. Salient points are as follows:

(a) Using currently accepted regimes of ultrasonic cleaning of PCBs (i.e. a few minutes at 11 watts/litre, no damage has been encountered with the range of electronic components studied.

(b) Using abnormally high power densities (i.e. about three times that normally used) damage can be induced in some cases but only after more than 10 minutes exposure time (usually much longer).

(c) Using abnormally long ultrasonic exposure times (about 100 hours at standard power densities), damage can be induced in some components.

(d) In all cases the observed damage was of a purely mechanical nature due to fatigue, and is located on the device bond-wire and/or the package legs.

(e) Ultrasonic cleaning using a CFC-based solvent under standard conditions of power density and time, is readily achieved within two minutes, even with standoff heights below 0.001 inch.

6.0 Task 2 Investigation

6.1 Equipment and Components Used

The same cleaning units used in Task 1 were again employed, but the solvents were as follows:

Aqueous Again, since the primary topic was the study of damage accumulation and not of cleaning, only one saponifier was used (Synperonic NP12). Owing to the poorer acoustic coupling properties of the water, the maximum power density obtainable with the Kerry equipment was 22 watts/litre.

Semi-aqueous The solvent chosen was the DuPont hydrocarbon material Axarel 38, considered by many people to be a potential direct FC replacement for cleaning PCBs. The power density required to clean boards was 24 watts/litre.

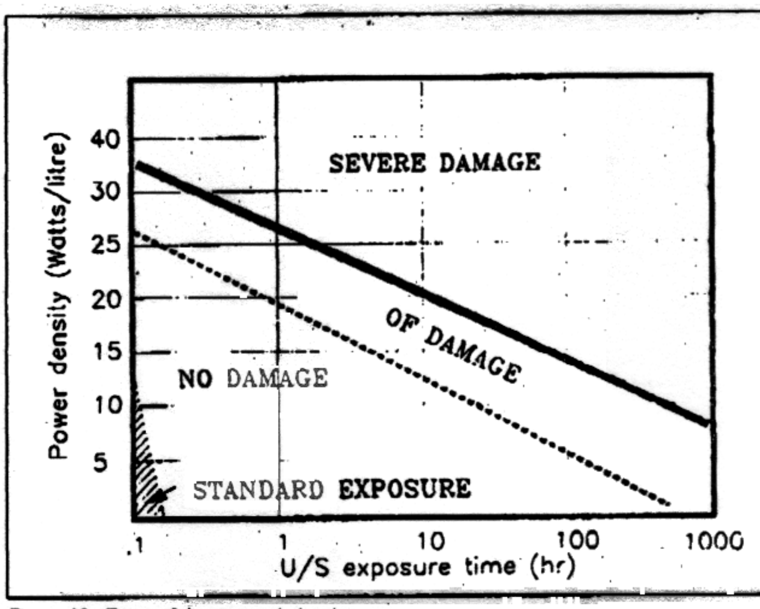

Figure 15 Zones of damage and cleaning

The components studied and the assessment techniques employed were chosen from those already discussed above.

7.0 Task 2 Results and Discussion

At this stage Task 2 is on-going: all the results have not yet been obtained, and those that are available have not yet received full interpretation. However, the early results are encouraging and the general trends give good support to those obtained using CFC solvents.

7.1 Aqueous Solvents

The effects of cavitation-induced damage to the components, although not serious, were more pronounced than those observed when using CFC solvents. For example, the metal lids of some ceramic components on the test boards displayed a cosmetic pattern of surface asperities.

Table 1 Summary of Results of Failure Mechanisms as a Function of Package Type

	Plastic					Ceramic				Metal	Other	
	DIP	SM	SM LED	SOT-23 A1	SOT-23 A6	4116	4001	68000 DIP	68000 PGA	TO-18	SM Resistor	SM Capacitor
Bond Wire H	N/A	N/A	N/A	N/A	N/A	0% 0.5 hr 5% 100 hr	0% 100 hr	1% 10 min 5% 100 hr	0% 1 hr 6% 20 hr	mounted—2% 40 hr loose—28% 100 hr	N/A	N/A
Bond Wire L	N/A	N/A	N/A	N/A	N/A	—	—	0% 124 hr	0% 124 hr	0% 27 hr	N/A	N/A
Leg H	34% 4 hr	1% 8 hr	1% 10 min 74% 15 hr	0% 0.5 hr 16% 15 hr	0% —0.5 hr 80% 15 hr	—	—	—	0% 100 hr	0% 100 hr	0% 100 hr	0% 100 hr
Leg L	0% 4 hr	0% 8 hr	0.5% 124 hr	0% 124 hr	0% 124 hr	—	—	—	0% 24 hr	0% 27 hr	0% 124 hr	0% 124 hr
Hermeticity H	N/A	N/A	N/A	N/A	N/A	10 hr	>100 hr	30 hr	30 hr	>100 hr	N/A	N/A

H = High power density 32 watts/litre
L = Low power density 11 watts/litre

7.1.1 TO-18 Transistors

These devices have been stressed both loose in a basket and mounted on boards for periods in excess of 50 hours at a power density of 22 watts/litre. Failures have been experienced for the loose devices, but the results are comparable to those expected from the Task 1 results with CFC solvents i.e. 1% failures within 2 hours. The individual results are shown in Figure 16 and compared with the earlier data. The slightly lower rate of accumulation of damage as compared to the CFC results is a direct reflection of the lower power density used.

During the course of this study another failure mode became apparent on some devices after approximately 10 hours exposure at the high power density. Some of the packages clearly failed as a result of cavitation-induced erosion and penetration of the can. The process originates in the production (or enhancement) of defects in the can plating, followed by ultrasonically-promoted corrosion of the underlying metal can, complete penetration of the can itself, and ingress of water and rust.

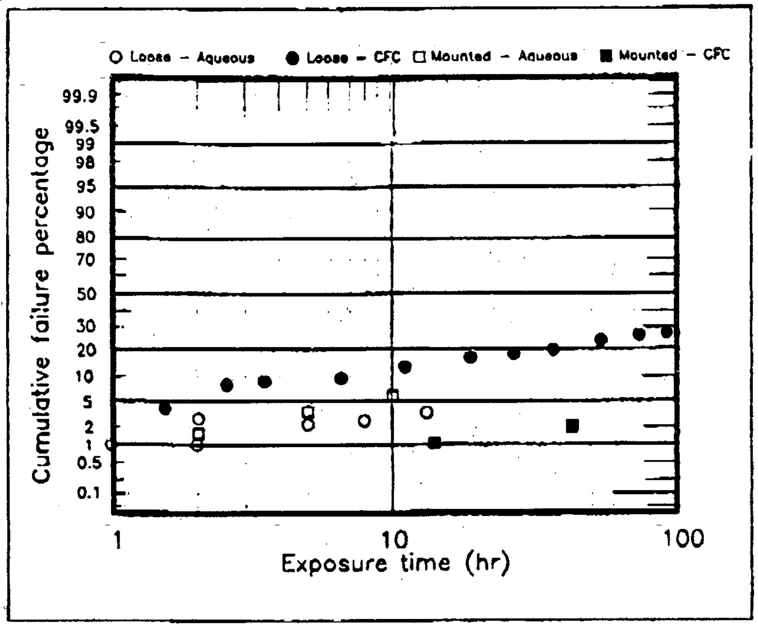

Figure 16 Failure of TO-can transistors at high power density

7.1.2 Plastic DIL Devices

The initial results on these devices (mounted on PCBs) have shown that although only 10 hours have yet been accumulated at high power density, no failures have been detected using optical and SEM appraisal techniques. The results appear better than those obtained using CFC solvents at 32 watts/litre.

7.1.3 Test Boards

These boards have been stressed for in excess of 10 hours at high power density, and in common with the plastic DIL devices no failures have yet been detected.

7.2 Semi-aqueous Solvent

A separate extensive exercise has been undertaken within GEC to evaluate the cleaning efficiency of the Axarel 38 using a range of boards (both test and production), and the Kerry Aquaclens cleaning equipment. The results, which will be reported elsewhere, have demonstrated that cleaning is achieved within 3 minutes using either ultrasonic agitation or cyclic dipping. In the light of those promising data, therefore, it was important that the possibility of damage accumulation be examined, and the same cleaning equipment has been used for this purpose. Although the tests using Axarel 38 have so far reached only 15 hours, they are continuing and will be terminated only when the exposure times exceed 100 hours.

7.2.1 TO-18 Transistors

A series of 100 transistors was stressed loose in a basket as described above. However, after a total of 15 hours exposure at a power density of 24 watts/litre there were no electrical (or optical) failures.

7.2.2 Test Boards

Test boards exposed for similar periods have again failed to produce failures as assessed optically.

8.0 Task 2 Interim Conclusions

The early results of this study of possible ultrasonic damage using aqueous or semi-aqueous solvents, have done nothing to dispel the encouraging view based on the results using CFC solvents. The preliminary data indicate that the type of damage and its accumulation are no worse than those associates with CFC solvents. The large margin of safety when employing currently accepted regimes of cleaning, again appears to be operative.

Acknowledgment

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